

VLSI Circuit Design Processes

VLSI Design flow:-

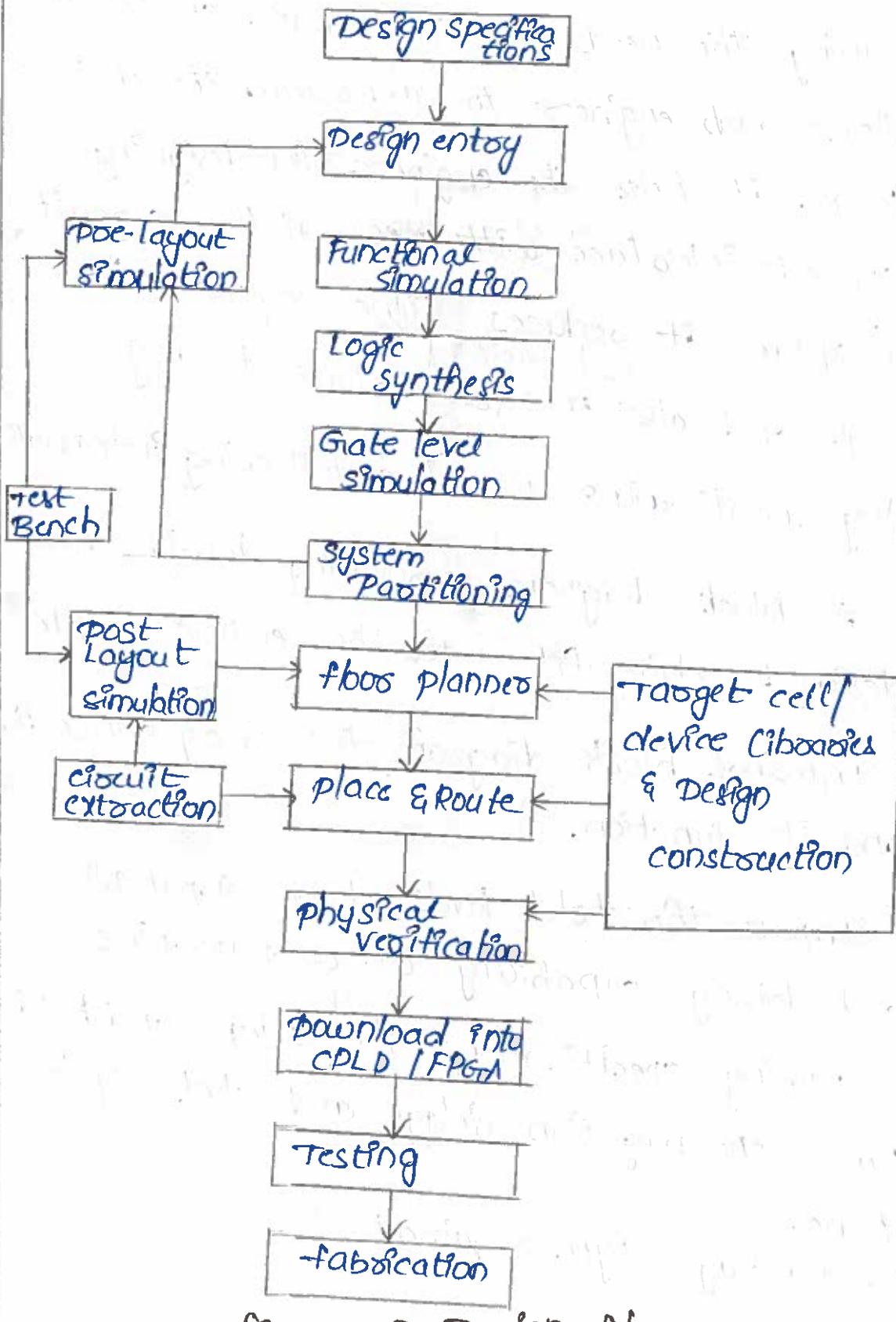


fig : VLSI Design flow

(i) Design specifications:-

specification of a design is as a guide to choose the right technology and for knowing the needs of the vendor. specifications allows each engineer to understand the entire design. It helps the engineers for designing correct interface with rest of the circuit or system it reduces time required for design and also misassumptions of any.

Any specifications includes following information

1. A block diagram providing details how designed chip fit into the entire system.
2. Internal block diagram for every subsection and its function.
3. Input threshold levels of all input pins and driving capability of output pins.
4. Timing specifications like setup and hold times, propagation delays and clock - cycle time.
5. package type required

6. total gate count of the system under design.
7. total power consumption of the circuit.
8. test procedures for different tests.
9. total cost of the target design chip.

(ii) Design Entry:-

User can enter a design with a schematic editor or other text-based software tool, either a hardware description language (VHDL or VERILOG).

Schematic Entry:-

It provides a graphical interface for design entry. A design can be build by a user with individual gates or he can combine gates to create functional blocks.

HDL Entry:-

This entry supports mixed level description where gate and netlist constructs both are used along with functional descriptions.

(iii) Functional Simulation:-

It is the process where logic in the design is checked before user implements

it in a device. As the timing information is not available at this early stage of design flow, functional simulator tests the logic of design using unit delays.

iv) Logic synthesis:-

Here logic synthesis is used which produces Netlist (textual information) from synthesis process. Logic cells and their interconnections are described in detail in the Netlist. Netlist is an EDF (Electronic data interchange format.) file. Thus during synthesis behavioral information in the HDL file is translated into a structure netlist.

v) System Partitioning:-

System partitioning is the process of dividing a large & complex system into smaller modules.

vi) Postlayout Simulation:-

This is required for verification of a circuit design through software programs. Here stimuli is applied to design over a specific

time period and according, analyzing the respective from the model.

vii) Floor Planner:

The main function of floor planner is to estimate the required chip area that will be used for each standard cell (S) module design. Floor planner is a tool that lets user generate and edit hierarchical floorplans.

viii) Place and Route:

After design mapping, flow engine places and routes the design. All logic blocks, including the configurable Logic Blocks (CLB) and Input-Output Blocks (IOB) are assigned specific locations on the die at place stage.

In the route stage the logic blocks are assigned, particular interconnect elements on die.

ix) Circuit Extraction:

This process determines the resistances & capacitances of all the interconnections.

(x) Post Layout simulation:-

After physical place and route, this simulation is carried out while carrying out this simulation propagation delays of logic cells and interconnection delays of interconnect are taken into account. If post layout simulation results full-fiu. the design specifications, designer can proceed for chip finishing part.

(xi) Physical Verification:-

After placement and routing and full custom editing physical verification is carried out. It is the process of interpreting the physical layout data to determine whether it conforms to the electrical design rules, physical design rules and source schematic. Design Rule check (DRC), Electrical Rule check (ERC), Antenna check & short circuit check, are the processes which under physical verification.

(xii) Testing:-

During production of chips, it is necessary

to have some sort of built-in test for designed system which continuously tests the system over long period of time. chip will fail because of some electrical or mechanical problems that will usually show up with such testing procedure.

XIII) chip fabrication:-

Before submitting design for fabrication top-o/p pads should be included in the design and its connectivity should be verified. Then appropriate package selection for the design and selecting bonding plan for the package is required. Details of how each pad of design is connected each pin of package is required.

Layouts:-

Mos design is aimed at turning a specification into masks for processing silicon to meet the specification. Mos circuits are formed on four basic layers - n-diffusion,

p-diffusion, polysilicon and metal, which are isolated from one another by thick (δ) thin silicon dioxide insulating layers. The thin oxide mask region includes n-diffusion, p-diffusion, and transistor channels. Polysilicon and thinox regions interact so, that a transistor is formed where they cross one another. In some processes, there may be a second metal layer and also, in some processes, a second polysilicon layer. Layers may deliberately joined together where contacts are formed. We have also seen that the basic MOS transistor properties can be modified by the use of an implant within the thinox region and this is used in NMOS circuits to produce depletion mode transistors.

Bipolar transistors can be included in this design process by the addition of extra layers to a CMOS process. This is referred to as BiCMOS technology, and in this text it is dealt with in an n-well.

CMOS environment.

STICK DIAGRAMS

- * stick diagrams are used to convey layer information through the use of colour code.
- * to describe logic networks, it is convenient to use stick diagrams which help to visualize the function as well as the top topology of the network. This is particularly true for NMOS circuits.
- * A stick representation hides lower level circuit details and electrical parameters such as current, speed and noise, but comes one step closer to actual layout. It views the NMOS networks as an interconnection of wires in three layers denoted by the three colours red, green and blue, representing the layers polysilicon, diffusion and metal respectively.
- * other colours also define other features such as yellow for implant & black for contact cuts, in order that black and white

copies of stick diagrams do not lose the layer information.

* The complemented colour coding by monochrome encoding of the lines. The monochrome form is shown below. While drawing stick diagrams for own designs, single lines of appropriate colours are to be used.

* Colour coding is also applied to mask layout information and by hatched representation monochrome encoding of the same is also provided. Note that monochrome encoding schemes to diagrams and mask layout are readily reproduced by copying machines.

* One of the fundamental difficulties in specifying design rules is that the fabrication processes are undergoing rapid evolutionary changes. Hence the colour and monochrome encoding schemes too have evolved to cover NMOS, CMOS and BiCMOS processes and to be compatible with the design processes of GaAs.

* Stick diagram representation has all the

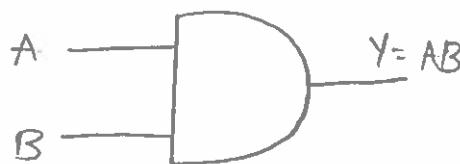
advantages and features that a designer fabrication interface requires. The layout given by stick diagrams faithfully represents the topology of the actual layout in silicon.

Logic gates Implementation using nmos,

Pmos & CMOS

Logic gates Implementation using nmos:-

2 i/p AND gate



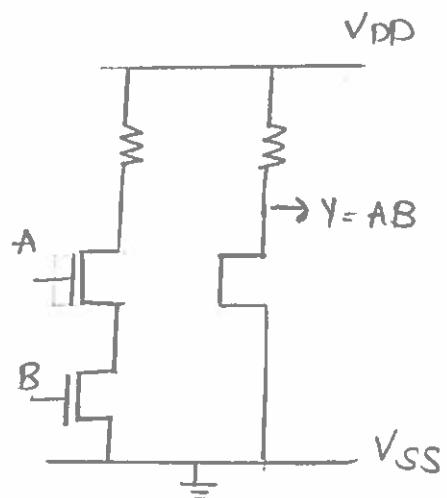
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0	0	0
0	1	0
1	0	0
1	1	1

2 i/p OR gate:-

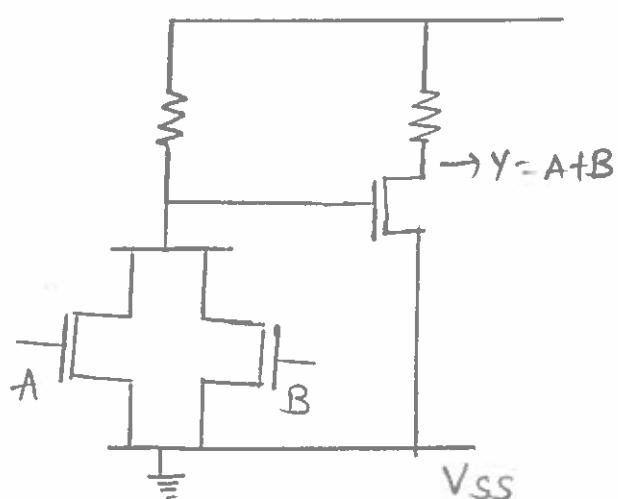


A	B	Y
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0	1	1
1	0	1
1	1	1

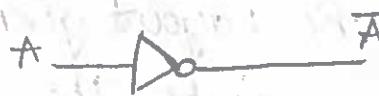
AND gate using nmos



OR gate using nmos

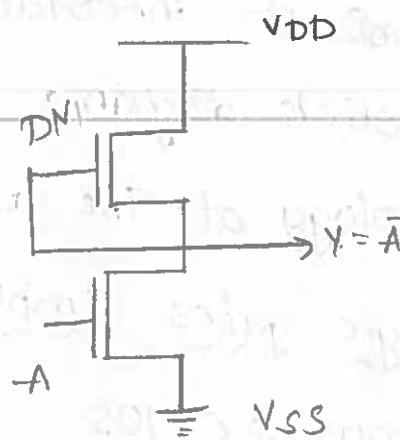


NOT gate

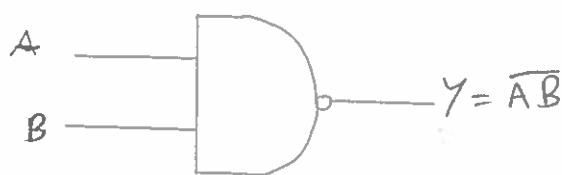


A	X
0	1
1	0

NOT gate using nmos

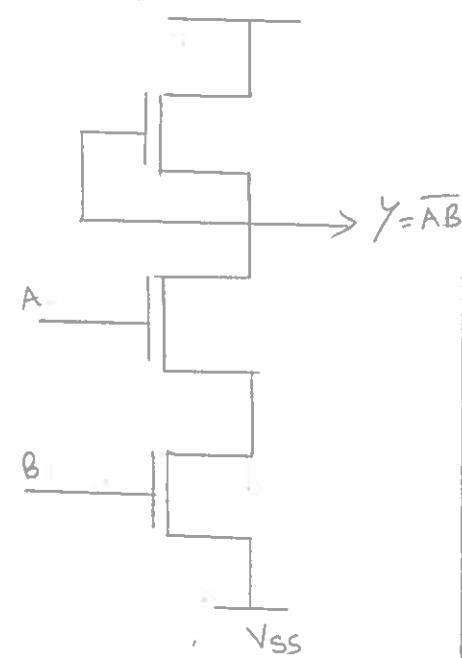


2-Input NAND gate

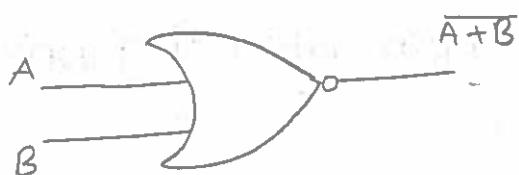


A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NAND gate using nmos

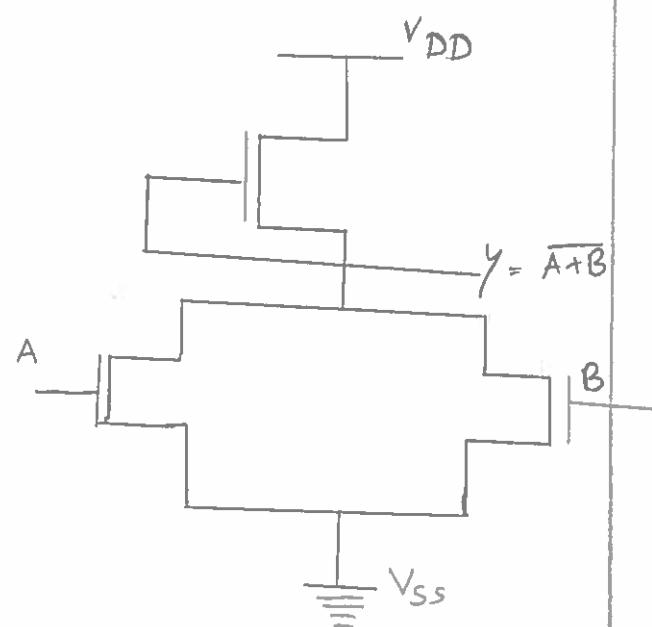


2-Input NOR gate

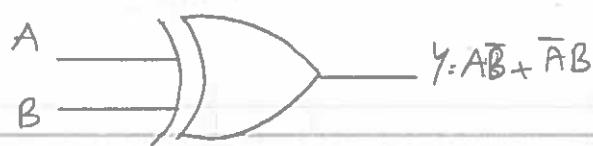


A	B	Y
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0	1	0
1	0	0
1	1	0

NOR gate using nmos

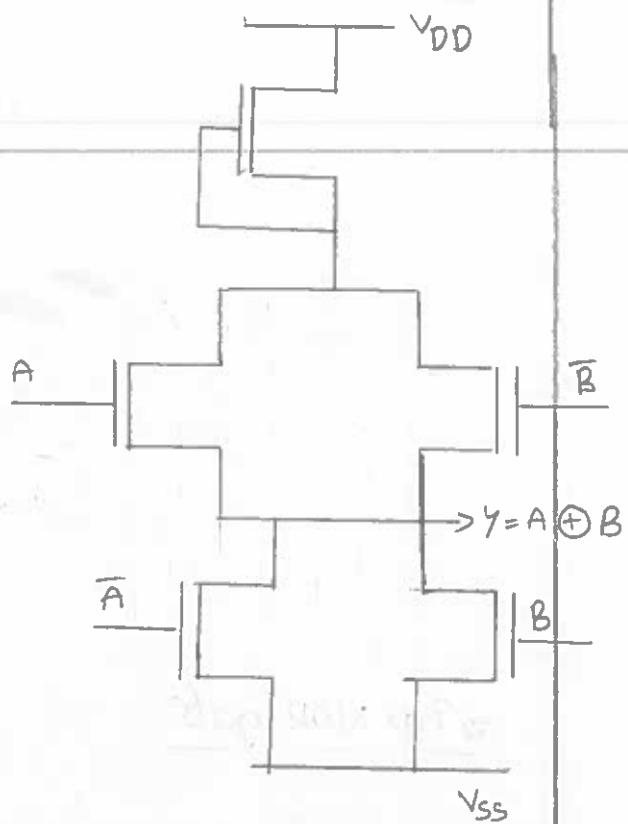


2 input XOR gate



A	B	Y
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0	1	1
1	0	1
1	1	0

XOR gate using nmos

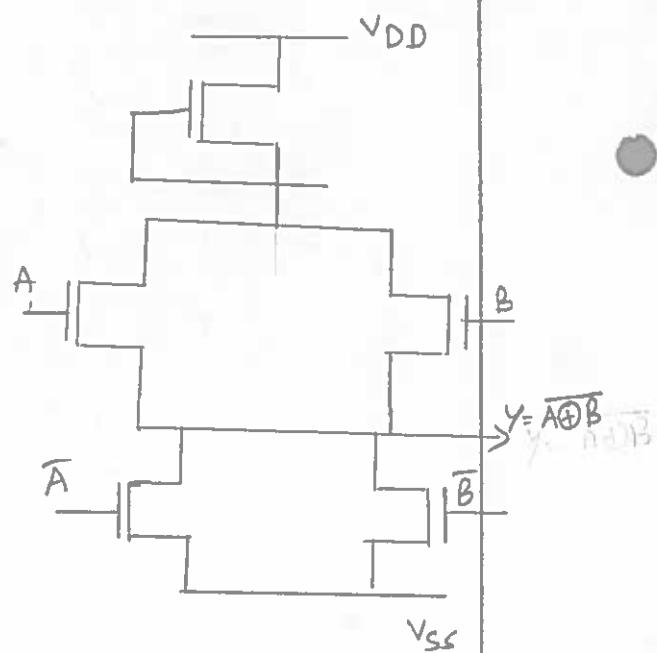


XNOR gate

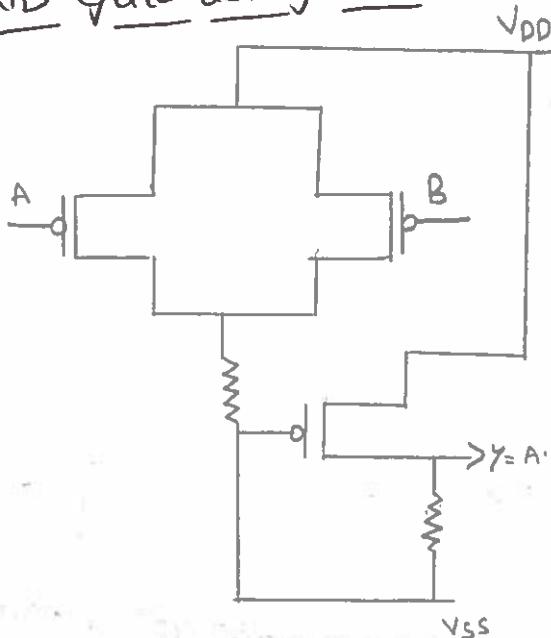


A	B	Y
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0	1	0
1	0	0
1	1	1

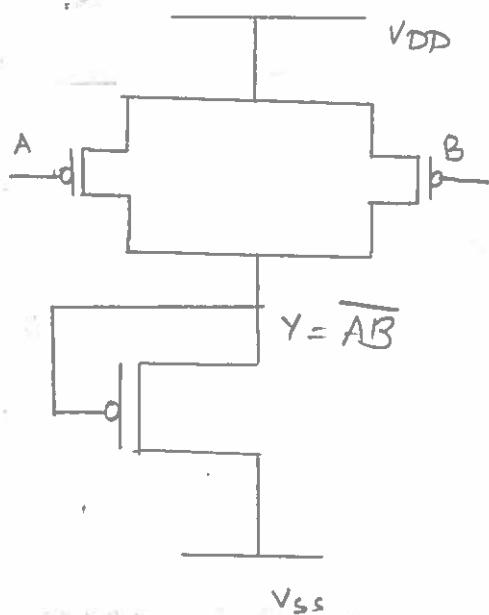
XNOR gate using nmos



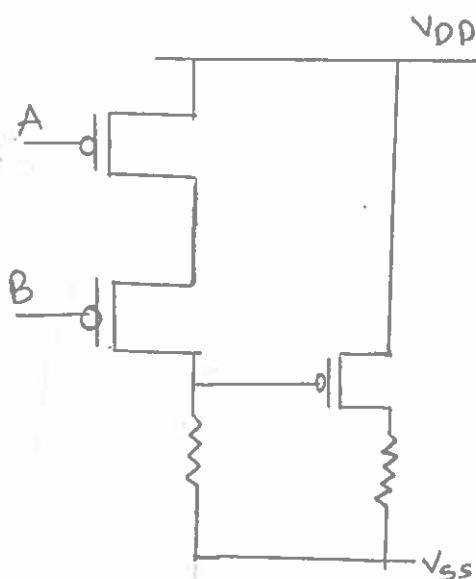
PMOS
AND gate using PMOS



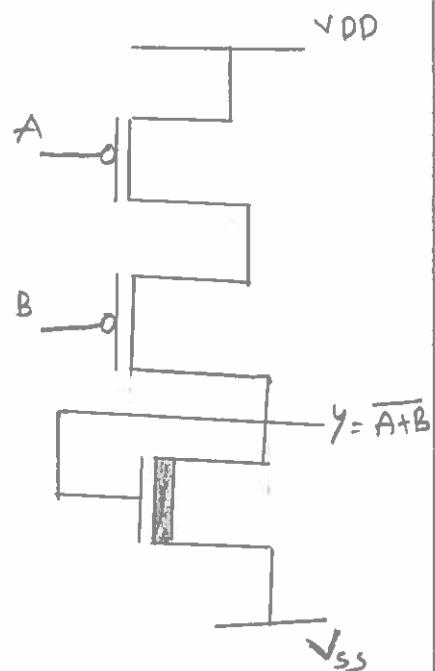
NAND gate using PMOS



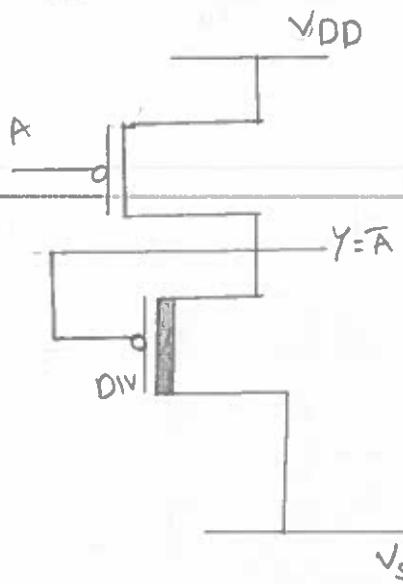
OR gate using PMOS



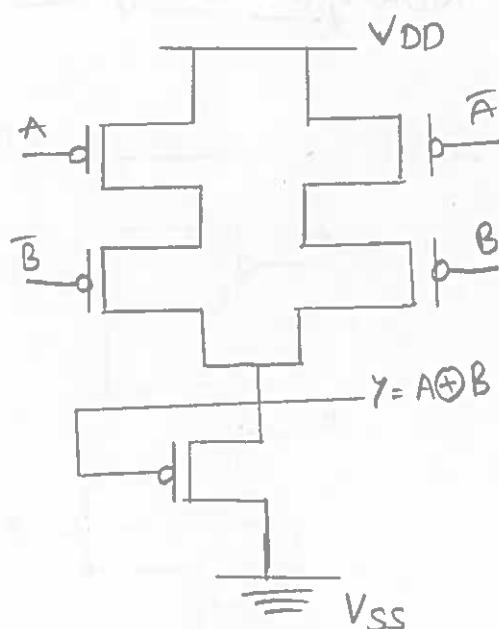
NOR gate using PMOS



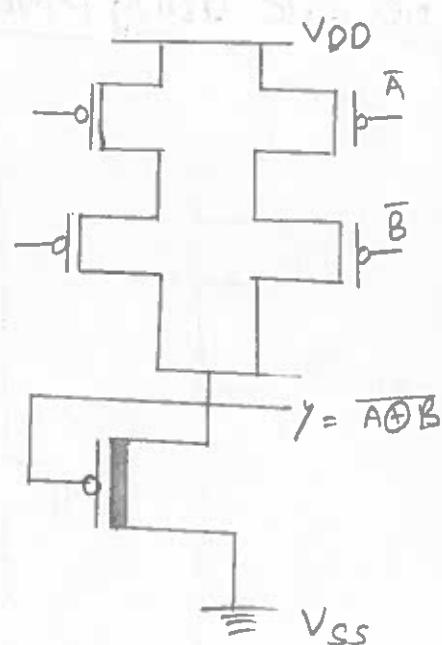
NOT gate using PMOS



X-OR gate using PMOS

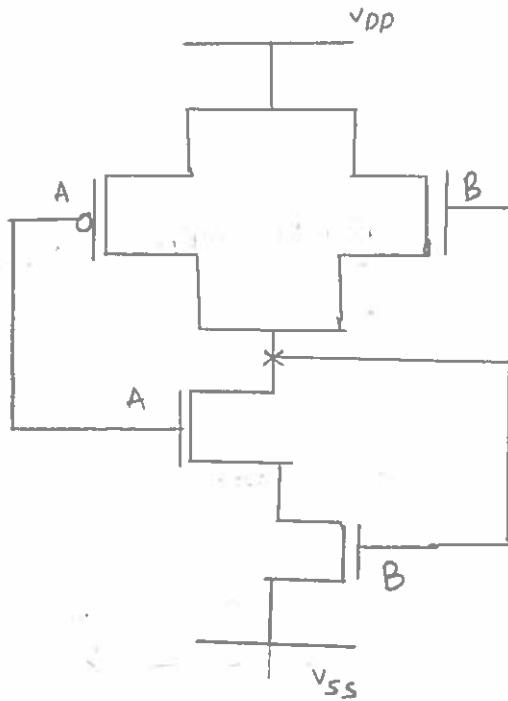


X-NOR gate using PMOS

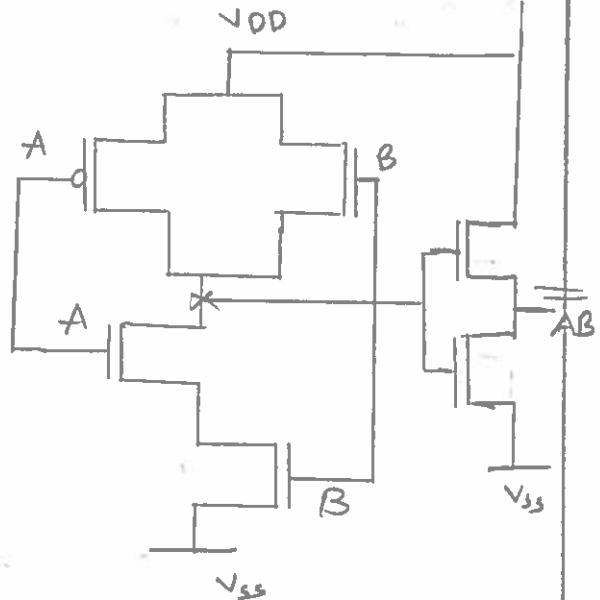


Q

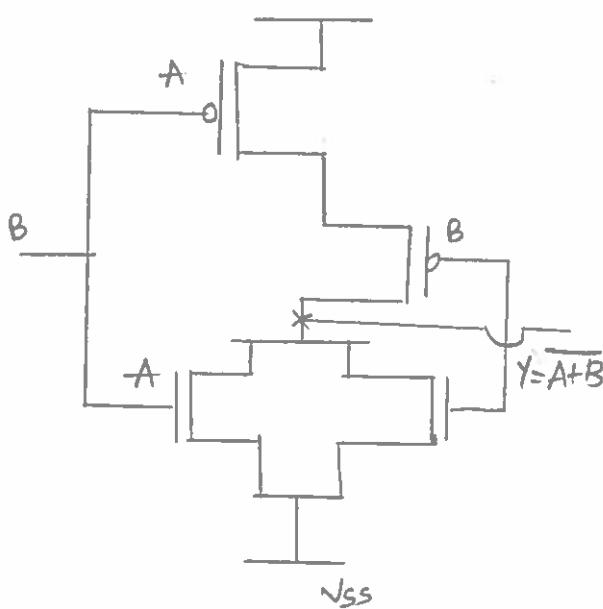
CMOS NAND gate using CMOS



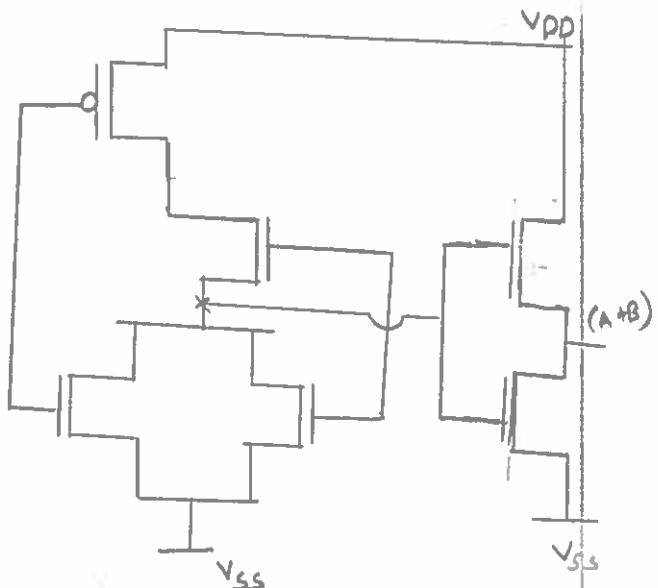
AND gate using CMOS



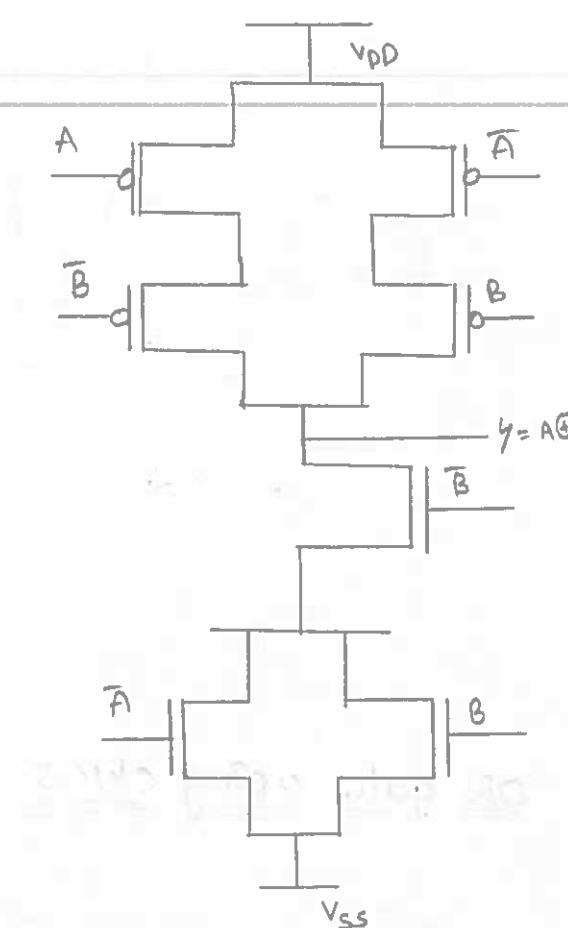
NOR gate using CMOS



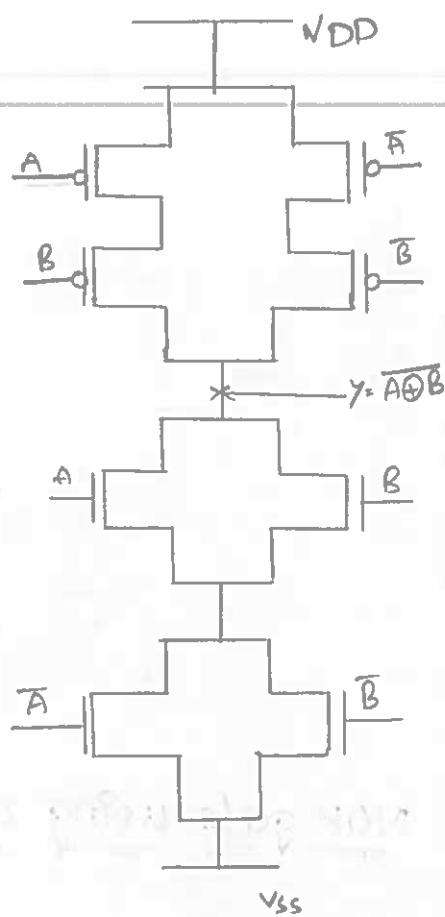
OR gate using CMOS

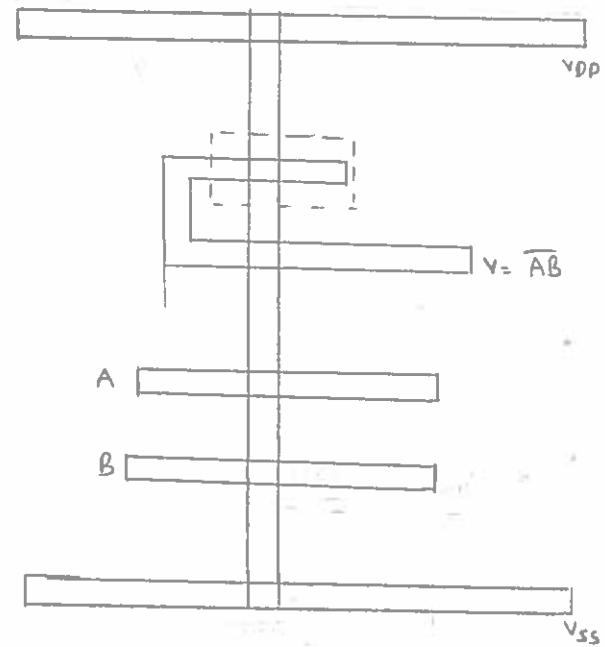
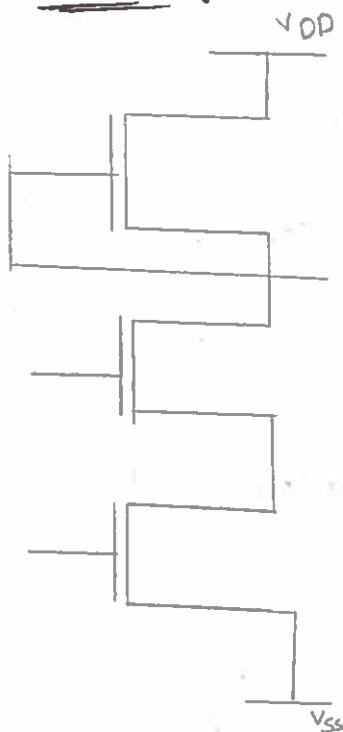
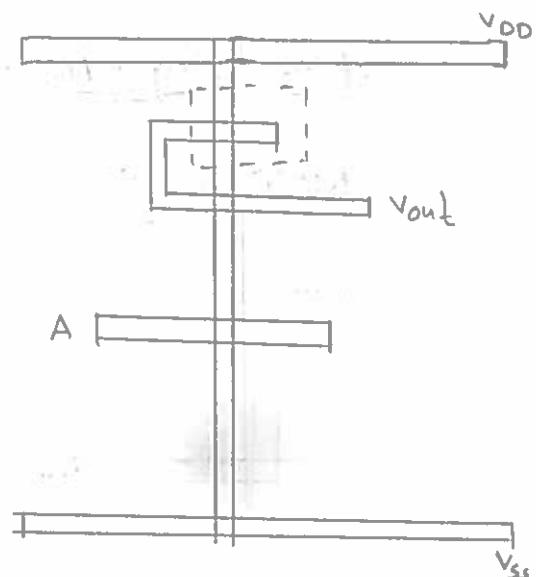
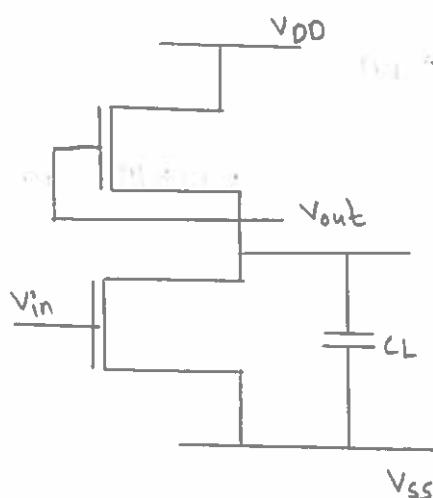


XOR gate using CMOS

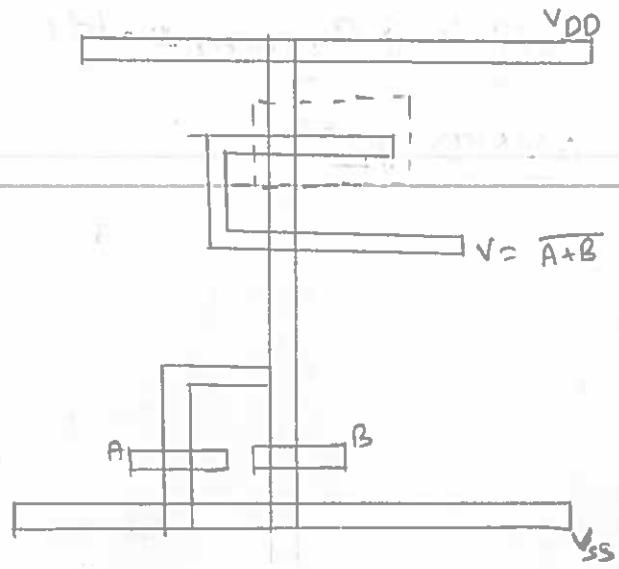
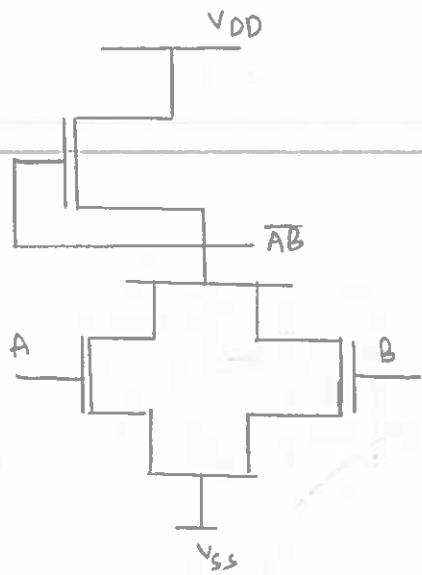


xNOR gate using CMOS

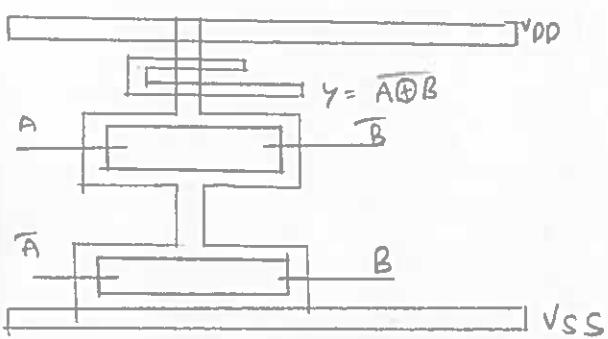


STICK DIAGRAMSstick Diagrams for NMOSNAND gateNOT

NOR

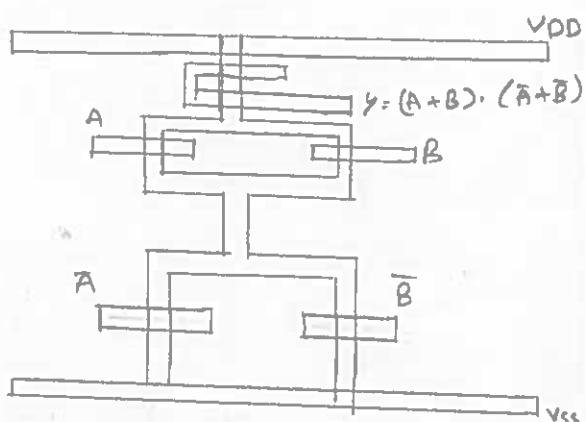


XOR NMOS

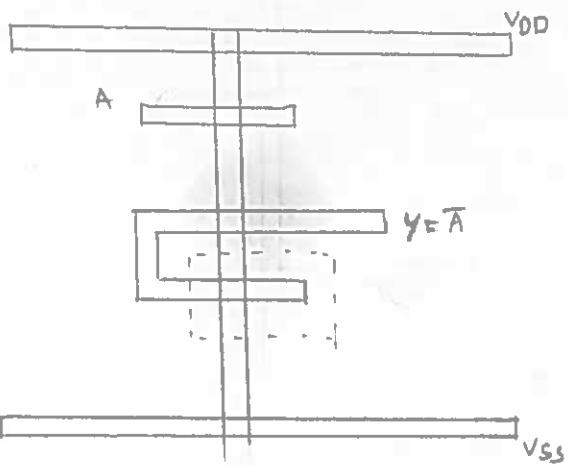


stick diagrams for

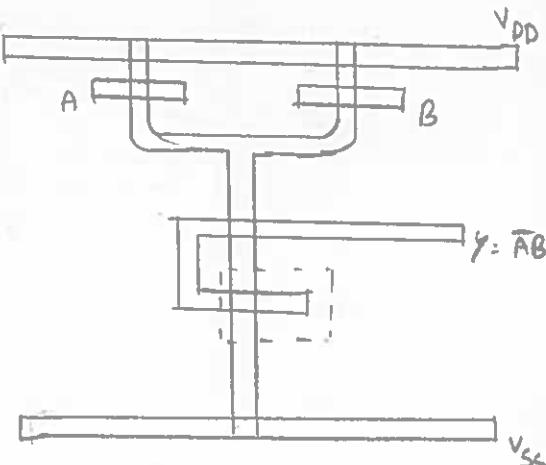
XNOR NMOS

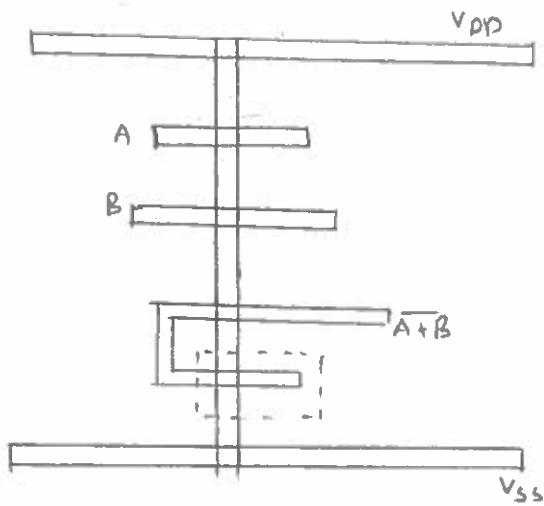
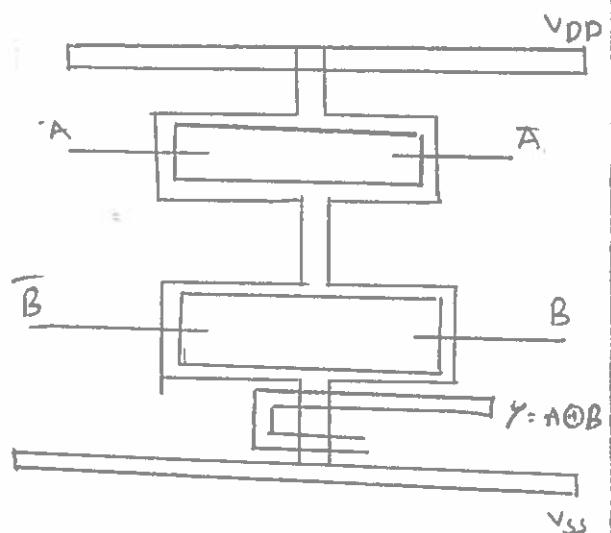
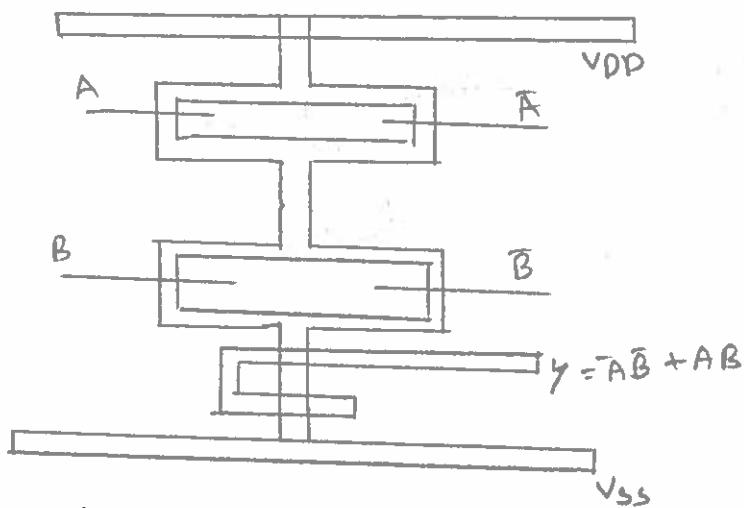
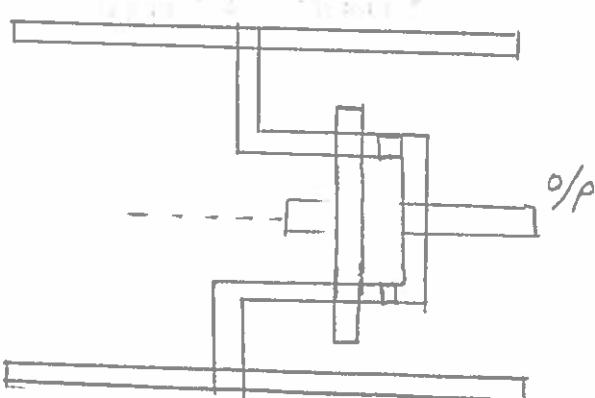
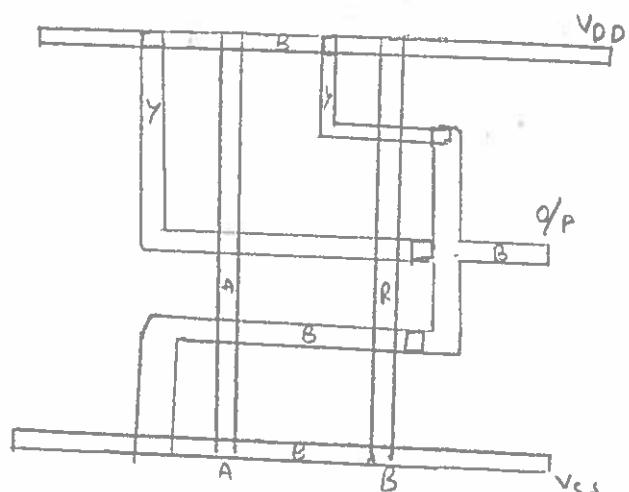


NOT gate

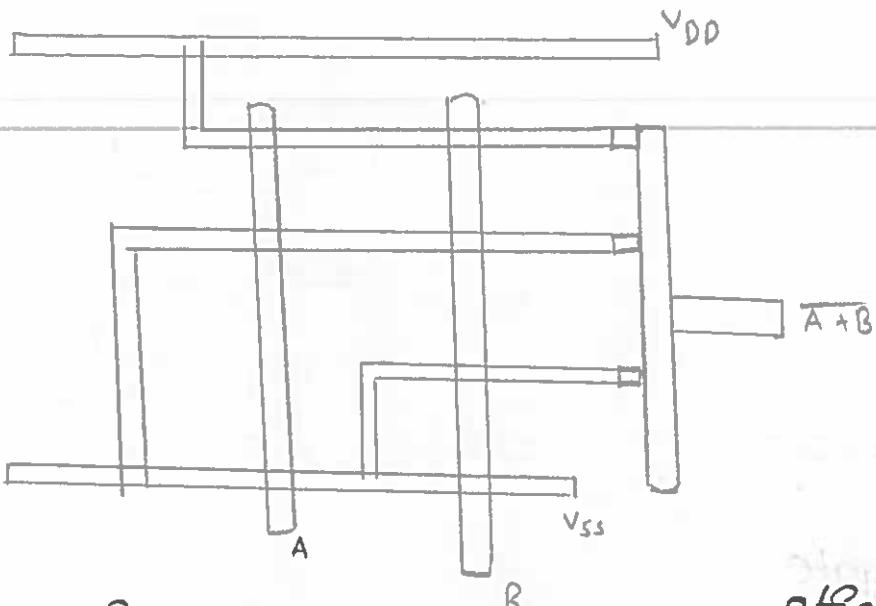


NAND gate

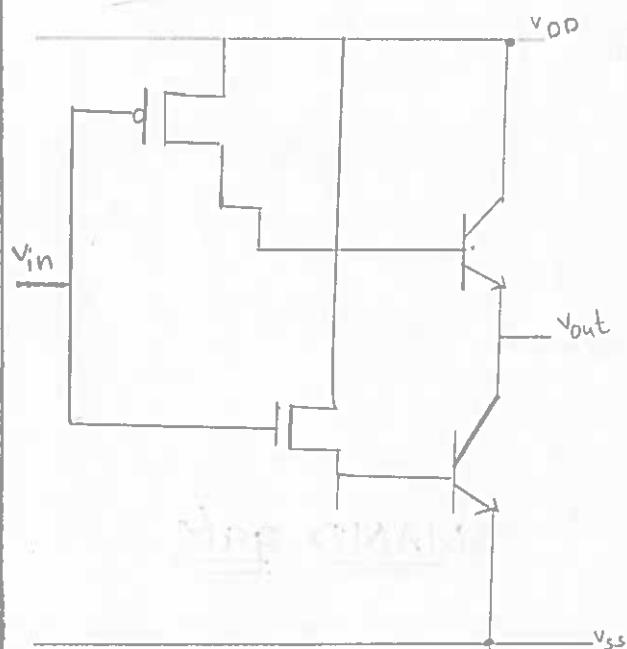


NOR gateXOR gateXNOR gatefor CMOS
NOT gateNAND gate

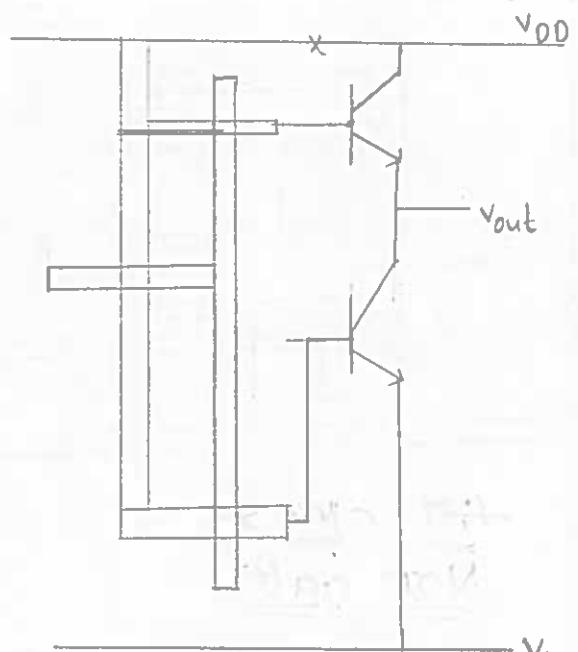
NOR gate



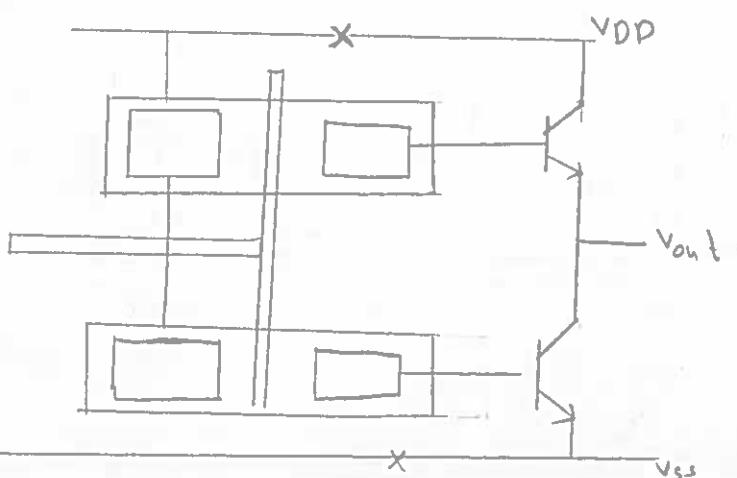
BICMOS

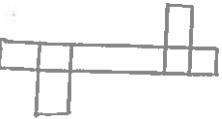
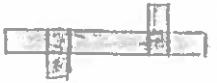
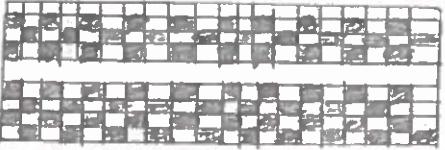


stick diagram



Layout



color	stick Encoding	Layers	Mask layout
Green		[n-diffusion cnt active TiNox*]	Mono CHROM 
RED		polySilicon	
Blue		Metal 1	
Black		contact cut	
Grey	Not applicable	overglass	
nMOS only YELLOW		Implant	
nMOS only BROWN		Buried contact	

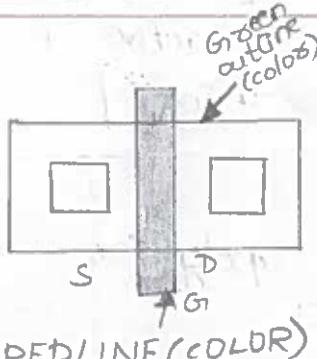
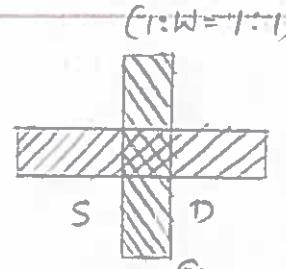
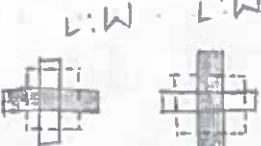
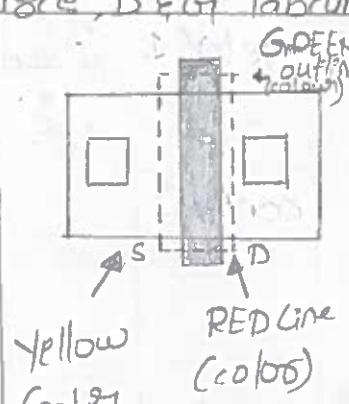
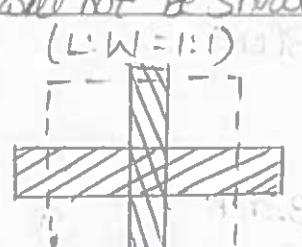
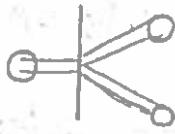
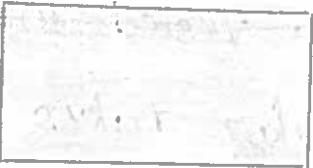
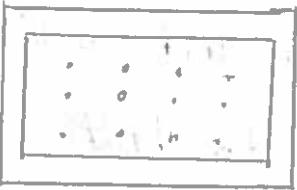
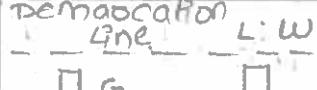
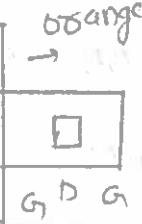
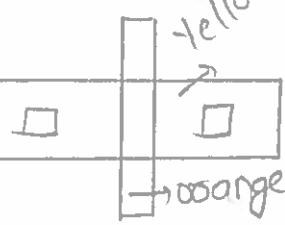
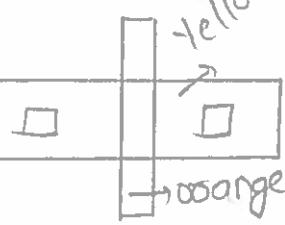
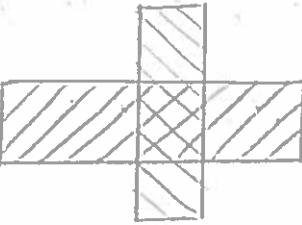
feature	feature (STICK) MONOCHROME	feature (symbol) (monochrome)	feature (Mask) (monochrome)
n-type enhancement mode transistor	L:W 		
n-Type depletion mode transistor Nmos only	L:W · L:W 		

fig: Encodings for a simple metal nmos process (see color plate 1(a) for nmos color encoding details.)

Double metal double poly BiCMOS n-well process

colour	stick encoding	Layers	Layout encoding	CIF layer
orange		poly _{Si2}		CPS
Brown & green		bipolar npn transistor		Not App
PINK	Not separately P-base of encoded	bipn transistor		CBA
PALE Green	Not separately encoded	buried collector of bipolar npn		CCA

Feature	Feature stick	Feature symbol	Feature (Mask)
n-type EM poly _a transistor	demarcation line  	  	
p-type em poly _a transistor	 	 	

Design Rules & Layout

The object of a set of design rules is to allow a ready translation of circuit design concepts, usually in stick diagram (B) symbolic form, into actual geometry in silicon. The design rules are the effective interface between the circuit/system designer and the fabrication engineer. Clearly, both sides of the interface have a vested interest in making their own particular tasks as easy as possible and design rules usually attempt to provide a workable and sellable compromise that is friendly to both sides.

Circuit designers in general want tight, smaller layouts for improved performance & decreased silicon area. On the other hand, the process engineer wants design rules that results in a controllable and reproducible process.

The following are the types of design rules & layouts.

Lambda-based design rules

In general design rules and layout methodology based on the concept of ' λ ' provide a process and feature size independent way of setting out mask dimensions to scale.

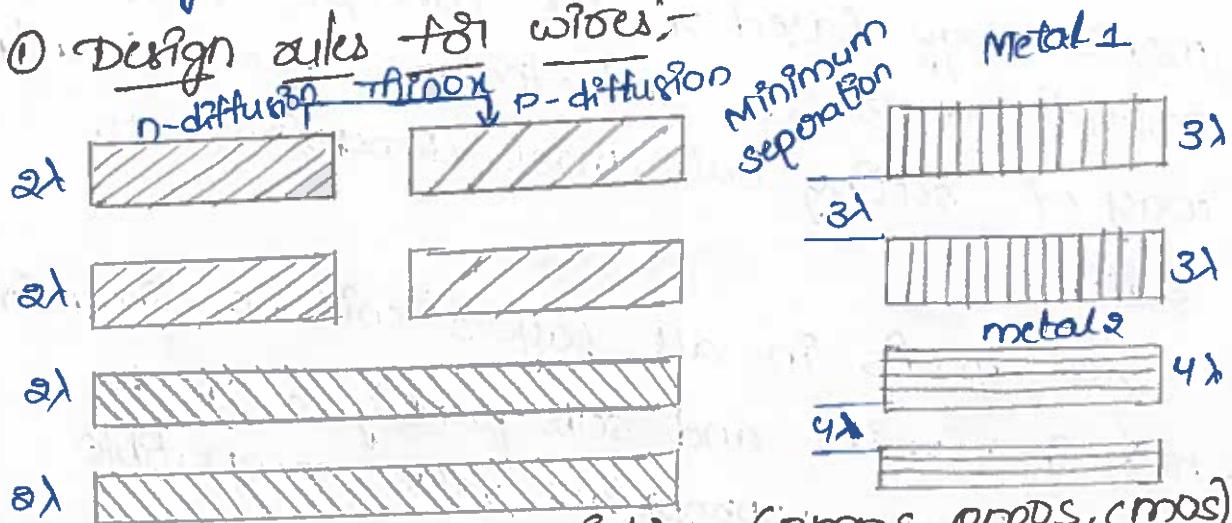
All paths in all layers will be dimensioned in λ units and subsequently λ can be allocated an appropriate value compatible with the feature size of the fabrication process.

This concept means that the actual mask layout design takes little account of the feature size, subsequently allocated to the feature, if design rules are correctly obeyed, the mask layout will produce working circuits for a range of values allocated to.

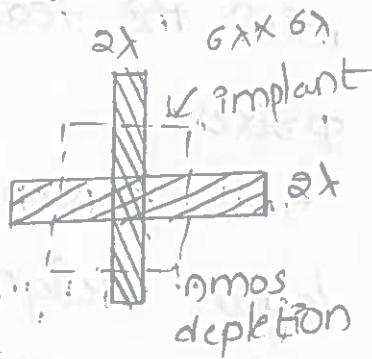
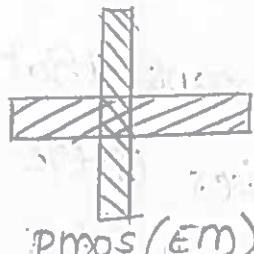
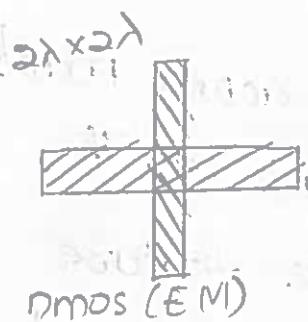
For ex:- λ value $1.0 \mu\text{m}$ so, that minimum feature size on chip will be $2\mu\text{m}$ (2 λ)

→ Design rules, also due to Mead and Conway, specify line widths, separations, and extensions in terms of λ , and are readily committed to memory.

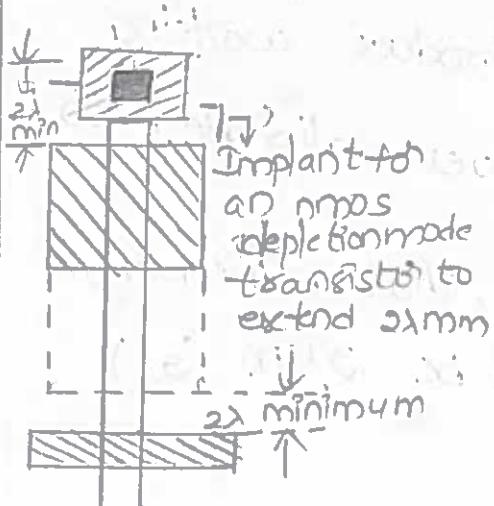
① Design rules for wires:-



② Design rules for Transistors (nmos, pmos, cmos)



separation from contact cut



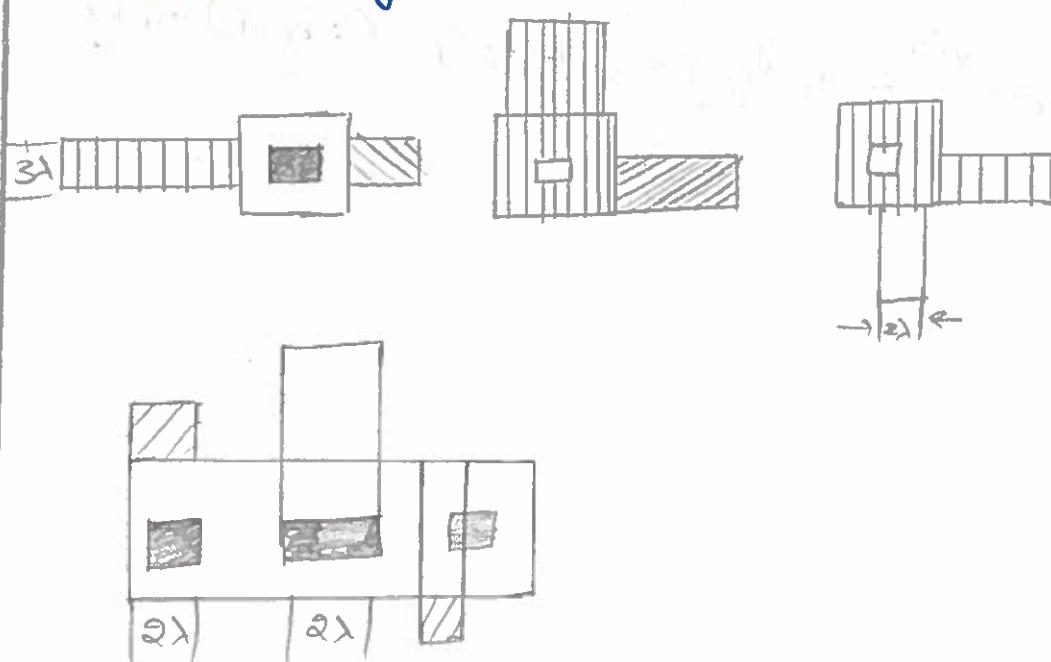
Contact cuts—(nmos, cmos)

When making contacts between polysilicon and diffusion in nmos circuits it should be recognized that there are 3 possible approaches.

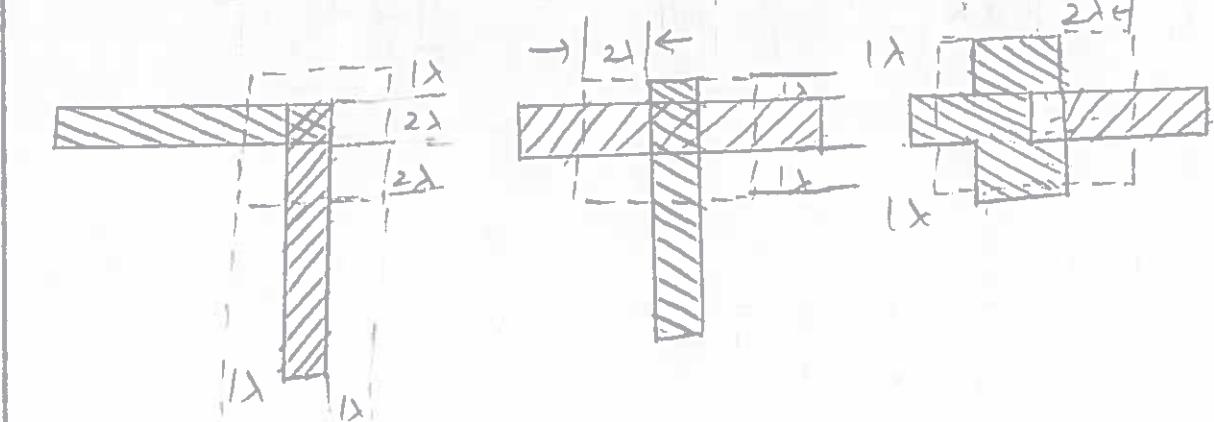
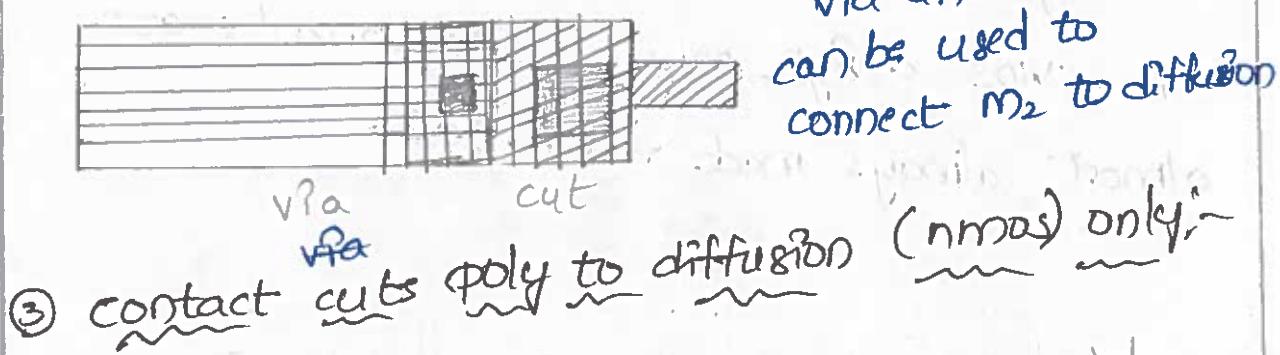
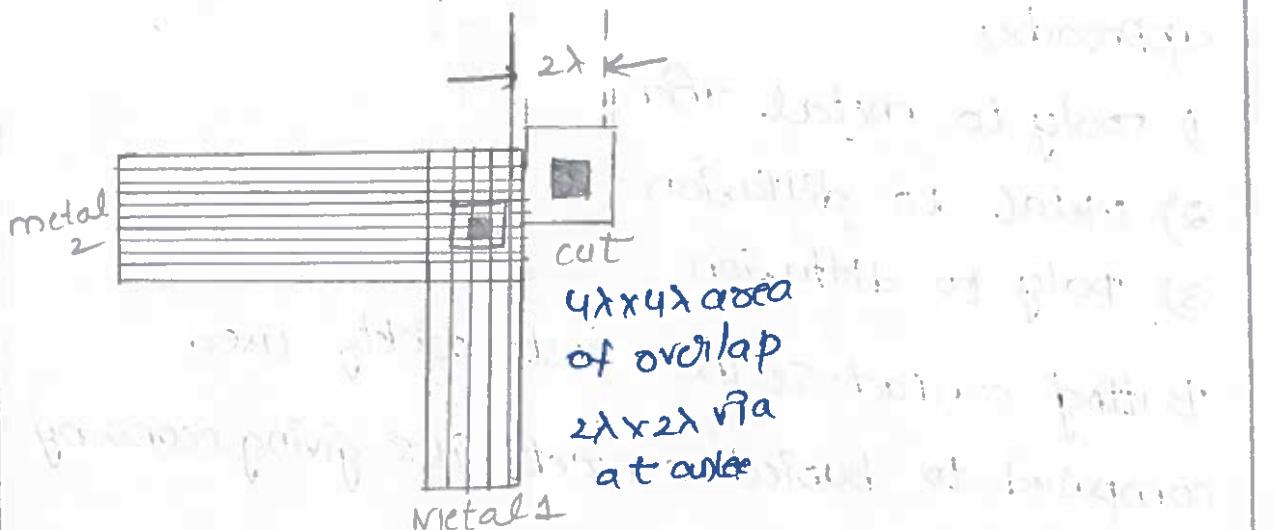
- 1) poly to metal then
- 2) metal to diffusion
- 3) poly to diffusion

Butting contact is the most widely used compared to buried contact its giving economy in space and reliable contact.

Butting contacts were widely used at one time. In cmos design, poly to diff. contacts are almost always made via metal.

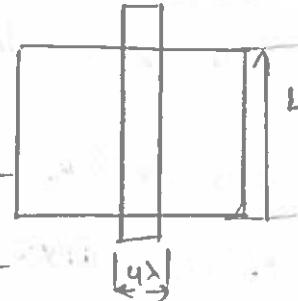


- (1) metal 1 to poly 81 to diffusion
- ② via (contact from metal 2 to metal 1
and thence to other layers)



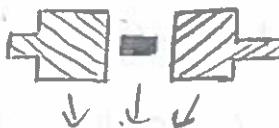


unrelated
poly or
diffusion

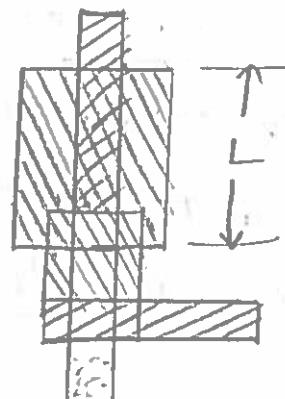
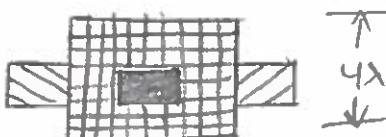


when nmos
is used as
pull up

3. Butting contact



It shows
without
metal lid
for clarity



Double Metal Mos Process rules

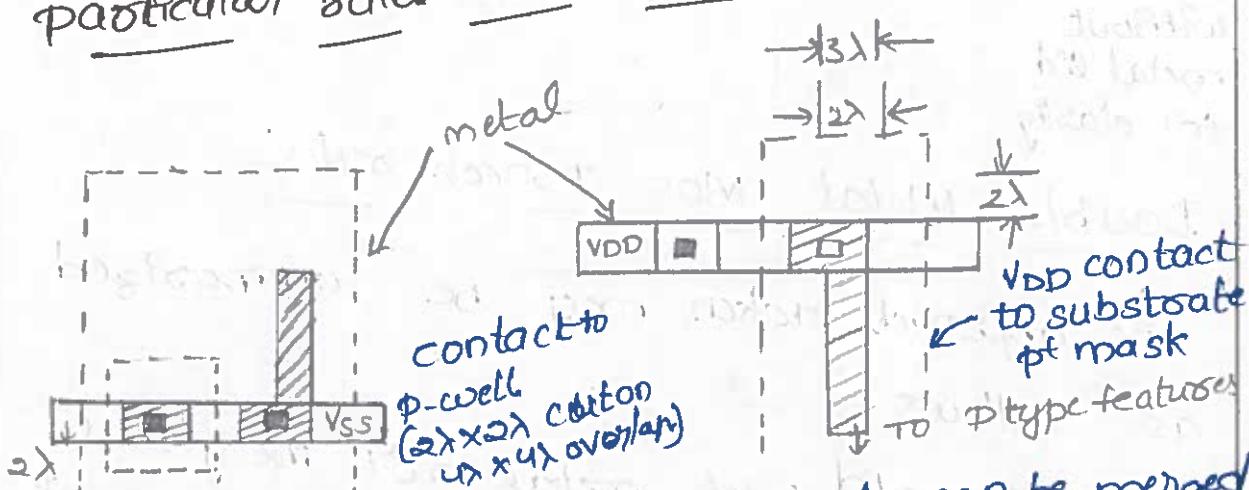
The approach taken may be summarized as follows

1. use the 2nd level metal for the global distribution of power buses, that is VDD and GND (VSS) and for clock lines.
2. use the first level metal for local distribution of power and for signal lines.
3. Layout the two metal layers so that conductors are mutually orthogonal whenever possible

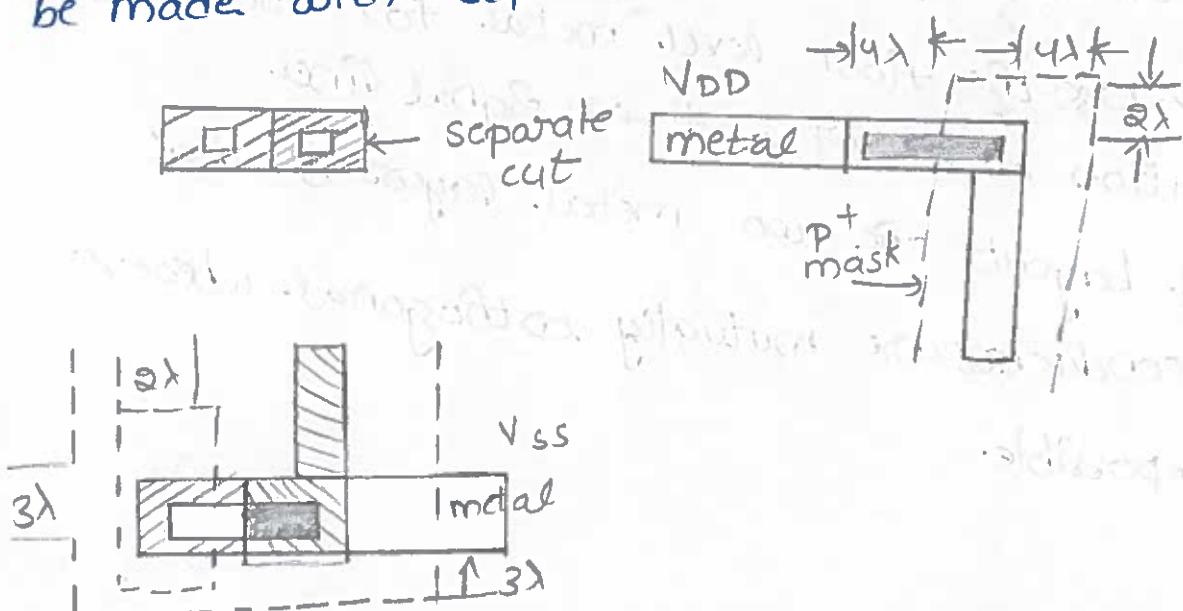
CMOS λ-based design rules:-

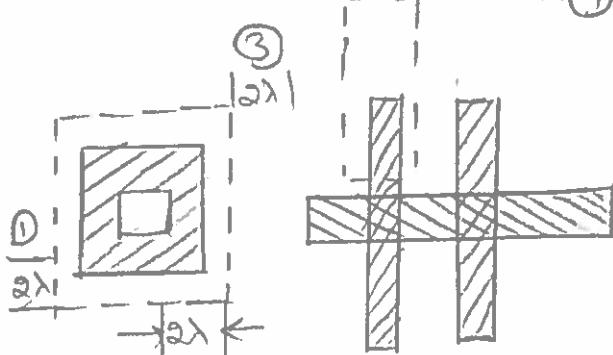
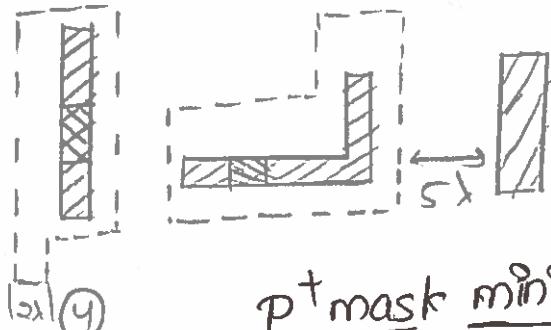
CMOS-fabrication process is much more complex than NMOS fabrication. The additional rules are concerned with those features unique to p-well CMOS, such as the p-well and p⁺ mask and the special substrate contacts.

particular rules for p-well CMOS process:-



Each of the above arrangement can be merged into single 'split' contacts; there also may be made with separate cuts.

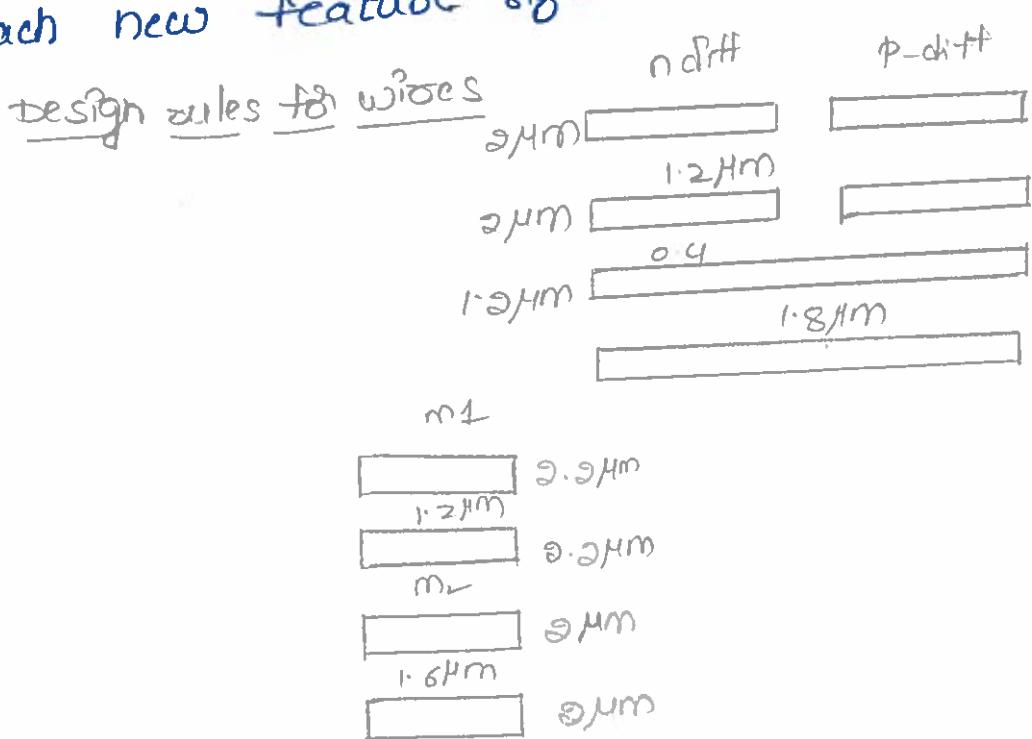


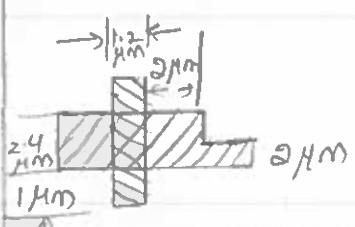


p+ mask minima

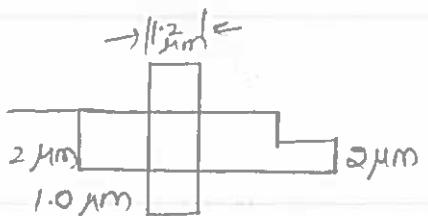
- ① overlap of $p+$ and $n+$
- ② separation to channel
- ③ separation $p+$ to $p+$
- ④ spacing from unrelated $p+$

1.2 μm double metal, single poly CMOS rules:
 As fabrication technology improves, so the feature size reduces, and a separate set of micron-based design rules must accompany each new feature size.

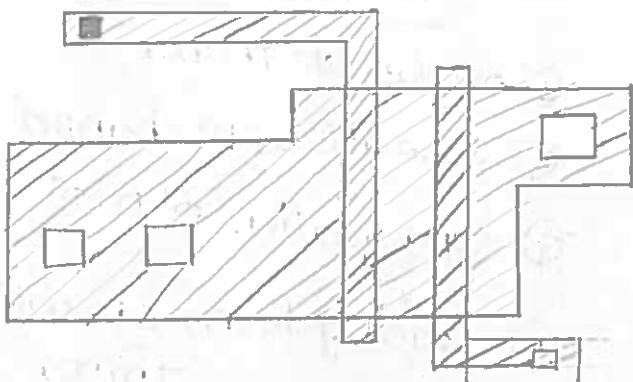




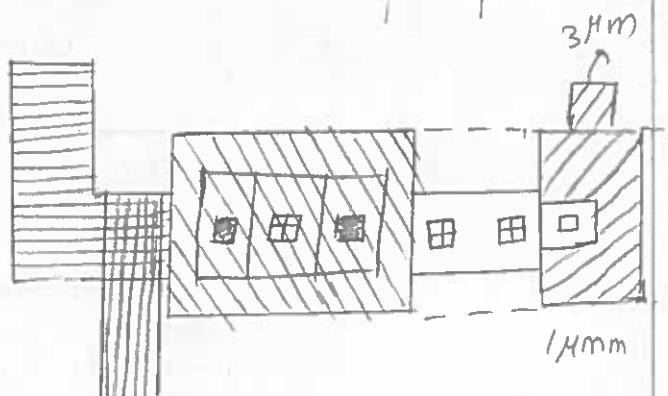
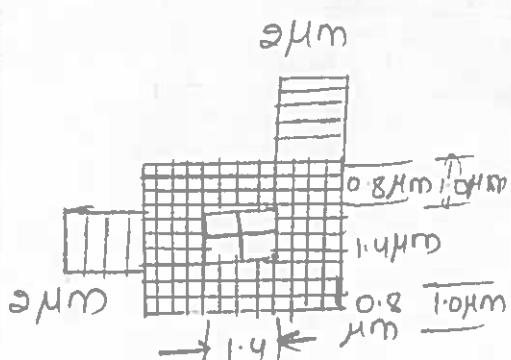
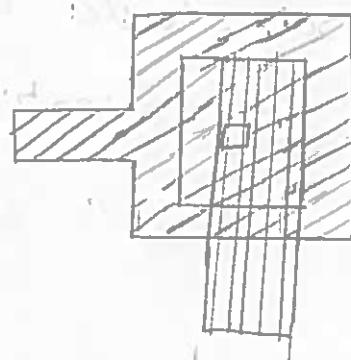
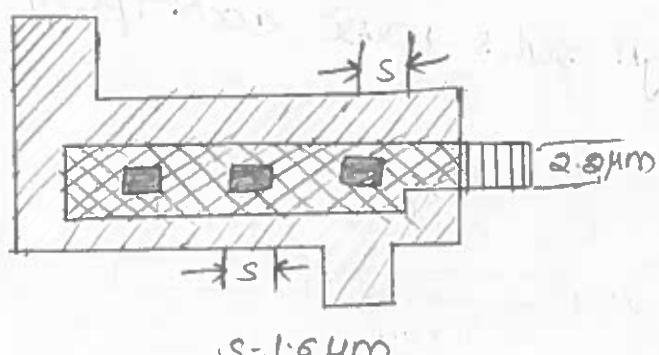
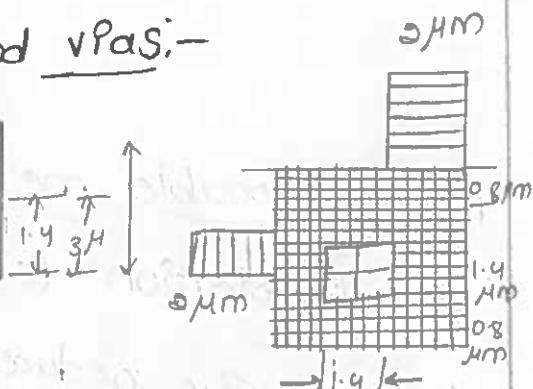
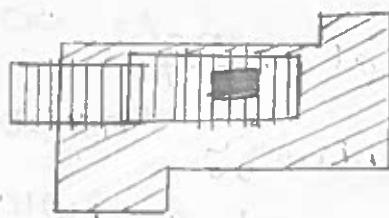
n-type e.m



p-type enhancement

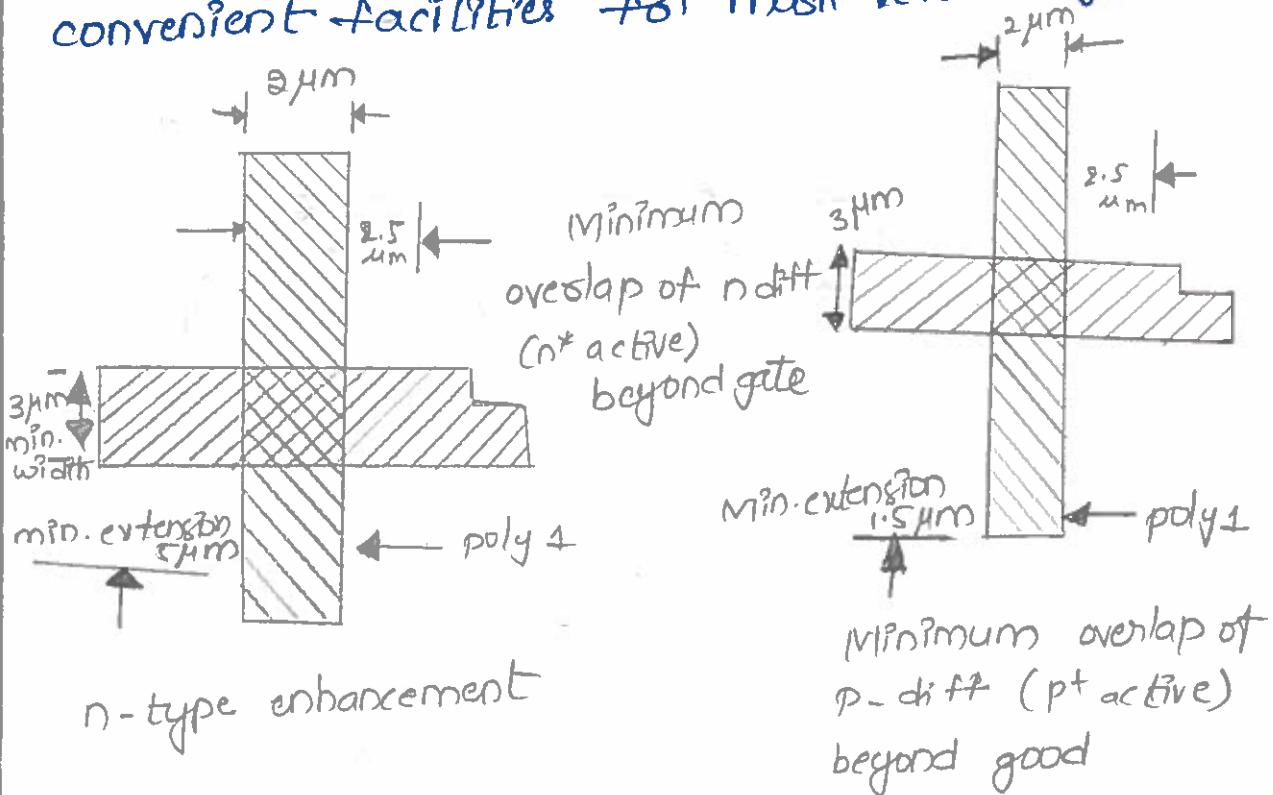


Rules for contact cuts and vPAs:-



Layout diagrams:- ($2\mu m$ Double metal, double poly CMOS / BiCMOS)

Mask Layout diagram may be hand-drawn on say, $5mm$ squared paper. In the case of Lambda-based rules, the side of each square is taken to represent λ and, for micron-based rules, it will be taken to represent the least common factor associated with rules (for example $0.25\mu m$ per side for the $0.4\mu m$ process and $0.2\mu m$ per side for the $1.2\mu m$ 8bit TM process layout). Most CAD VLSI tools also offer convenient facilities for mask level design.



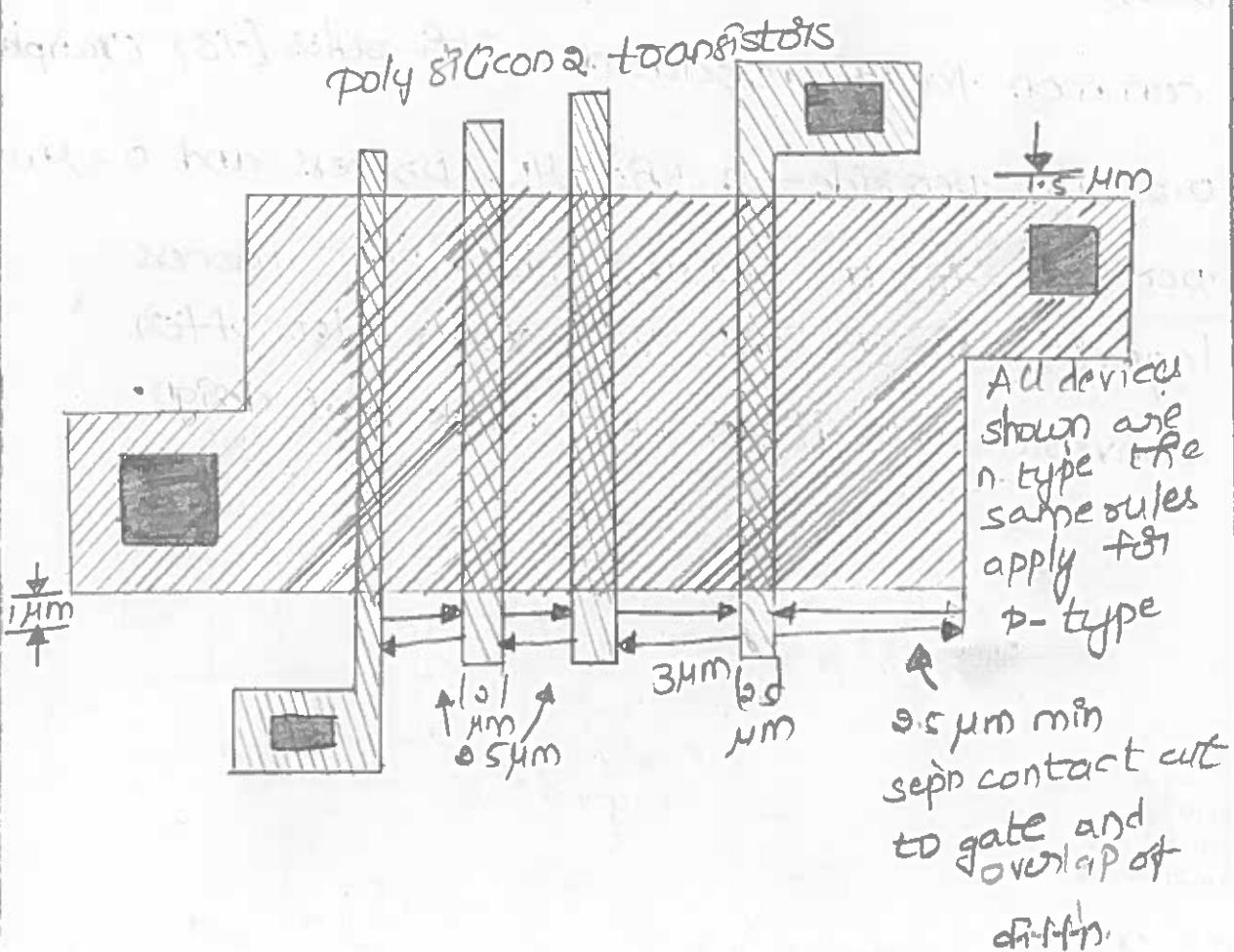
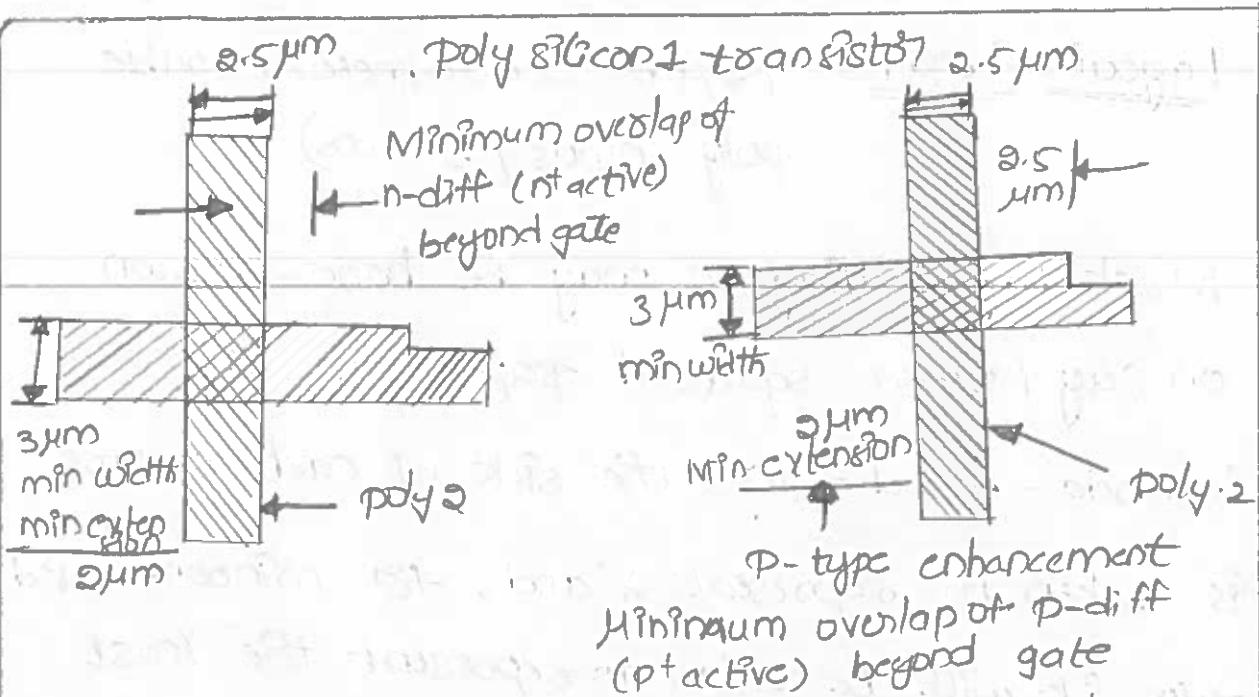
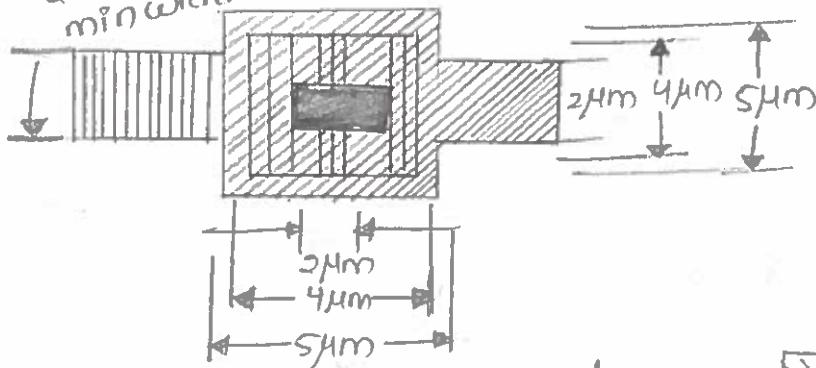


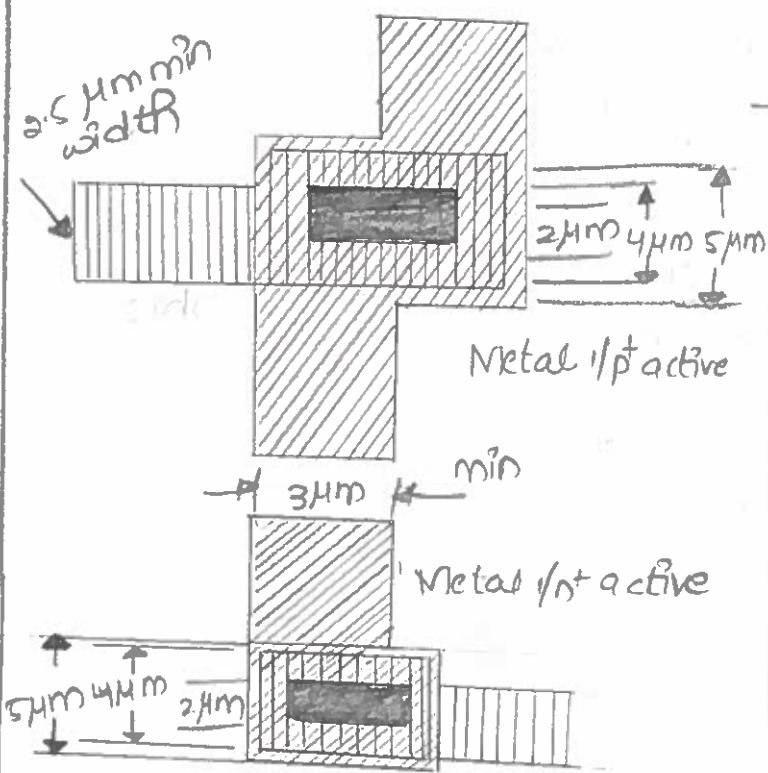
fig:- Rules for contact and vias (0.81μm CMOS)

2.5 μm min width



a) Metal 1 to poly 1(81) poly 2

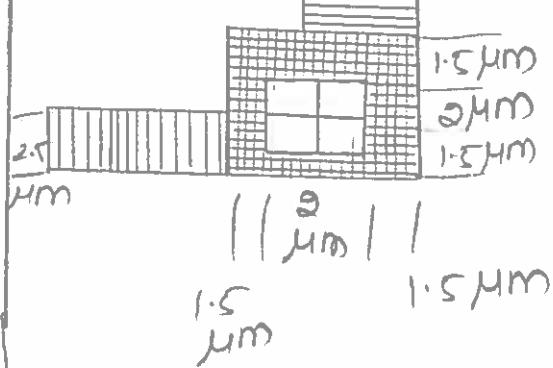
2.5 μm min width



(b) Metal 1 to n⁺ p⁺ active diffn

(c) via metal 1/3 μm

/metal 2



(e) Vias form metal 1 to metal 1 and thence to other layers.

